REMARKS/ARGUMENT

The applicant's attorneys appreciate the Examiner's thorough search and remarks.

Claims 3-5 and 7-8 have been cancelled without prejudice. Claims 1-2, 6 and 9-11 are pending in the application.

Responsive to paragraph 1 of the Office Action, applicant's attorneys are in the process of obtaining a better copy of the declaration and will submit the same in due course. It is respectfully requested that the objection set forth in paragraph 1 of the Office Action be held in abeyance.

Responsive to the objections set forth in paragraph 2, the Figures have been corrected. Approval of the corrections is requested. Withdrawal of the objections is requested.

Responsive to the objections set forth in paragraph 3 of the Office Action, Figures 2 and 5 have been corrected to show electrodes for the semiconductor die. The specification has been amended to properly identify the electrodes. No new matter has been added in that electrodes are inherent features of a semiconductor die. Withdrawal of the objections is requested.

Responsive to the objections set forth in paragraph 5, claims 1 and 9 have been corrected. Withdrawal of the objections is requested.

Responsive to paragraph 7 of the Office Action, appropriate amendments have been made. It is now believed that the claims satisfy section 112, second paragraph. Reconsideration is requested.

Claim 5 was rejected under 35 U.S.C. §103(a) over Nakanishi et al., U.S. Patent No. 5.793,108 in view of Adachi et al., U.S. Patent No. 4,993,148. It was set forth that Nakanishi et al. do not show an adhesive layer in combination with other limitations of claim 1. It was further set forth that Adachi et al. show using an electronically insulative material for an adhesive layer. Therefore, it was concluded that the combination of Nakanishi et al. and Adachi et al. makes the subject matter of claim 5 obvious to a skilled person in the art. Reconsideration is requested.

Claim 5 and its underlying base claims have been added to claim 1. Claim 1 now calls for, in combination with other limitations, a semiconductor device including a conductive pad and two die one of which is connected to a surface of the pad by a conductive adhesive and the other connected to the opposing surface of the pad by an electrically insulative adhesive. The

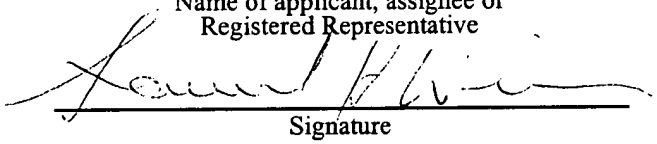
combination as set forth above is not suggested by Nakanishi et al., Adachi et al. or any other art of record. Reconsideration is requested.

Claims 2, 6 and 10-11 depend from claim 1 and therefore include its limitations. These claims include other limitations which in combination with those of claim 1 are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on July 11, 2002:

Samuel H. Weiner
Name of applicant, assignee or Registered Representative



Signature

July 11, 2002
Date of Signature

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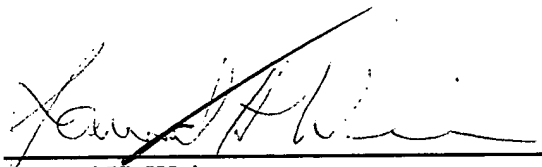
Respectfully submitted,



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APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Replacement for paragraph number [0023] at page 4:

[0023] In accordance with the invention, and as shown in Figures 1 and 2, the drain electrodes of two power MOSFET die 30 and 31 are conductively fixed to the opposite top and bottom surfaces of the lead frame 21. Thus, they can be connected by conductive adhesive layers such as layers 32 and 33 respectively in Figure 2. Layers 32 and 33 may be epoxies with silver particles loaded therein. Solder and tape can also be used. The first and second die are bonded so that they will not release from the lead frame during solder reflow. This arrangement connects the drains 30‴, 31‴ of each of MOSFETs 30 and 31 to a common drain node D (pad 21) as shown in Figure 4.

G1

Replacement for paragraph number [0024] at page 5:

[0024] The source electrodes 30′, 31′ on the opposite surfaces of MOSFETs 30 and 31 and the gate electrodes 30″ and 31″ on the same surfaces are then wire bonded to selected ones of the lead frame pins. Thus, sets of wire bonds connect the source electrode of die 30 to pins 22 and 23 while the gate electrode of die 30 is wire-bonded to pin 26.

Replacement for paragraph number [0031] at page 6:

[0031] In Figures 5, 6 and 7, parts identical to these of Figures 1 to 4 have the same identifying numeral. The IC die 50 is connected to the bottom of pad 21 by an insulation adhesive 51 (Figure 5) such as a polyimide or the like. The IC can derive its operating power from leads 23 and 27 and has a control input terminal connected to pin 26 and an output line 52 which is internally wire bonded to the gate electrode of die 30. The source electrode 30′ of die 30 may be wire bonded to one or more of pins 22 to 25.

G2

CLAIMS:

1. (Amended) A semiconductor device package comprising a lead frame having a conductive pad section with first and second opposite surfaces and a plurality of coplanar pin sections, a first and at least a second semiconductor die, each having first and second opposite surfaces at least one of said surfaces having a plurality of electrodes; said first surface of said first die being fixed to and connected with said first surface of said pad section; said first surface of said second die being fixed to and connected with said second surface of said pad section; an insulation housing enclosing said die and said pad section; a conductive adhesive for connecting said first surface of said first die to said first surface of said pad section; a second adhesive for connecting said first surface of said second die to said second surface of said pad section; wherein said second adhesive is electrically insulative; and wherein said pin sections extend through the surface of said insulation housing to its exterior.

G3

6. (Amended) The device of claim 1, wherein selected ones of said plurality of electrodes are connected to selected ones of said plurality of pins within said insulation housing

G4

9. (Amended) The package of claim 2, wherein said first and second die are MOSgated power devices; and wherein said first surfaces of said first and second die each contains a power electrode to be connected to said pad section and to one another.

G5

APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph number [0023] at page 4:

[0023] In accordance with the invention, and as shown in Figures 1 and 2, the drain electrodes of two power MOSFET die 30 and 31 are conductively fixed to the opposite top and bottom surfaces of the lead frame 21. Thus, they can be connected by conductive adhesive layers such as layers 32 and 33 respectively in Figure 2. Layers 32 and 33 may be epoxies with silver particles loaded therein. Solder and tape can also be used. The first and second die are bonded so that they will not release from the lead frame during solder reflow. This arrangement connects the drains 30‴, 31‴ of each of MOSFETs 30 and 31 to a common drain node D (pad 21) as shown in Figure 4.

Paragraph number [0024] at page 5:

[0024] The source electrodes 30′, 31′ on the opposite surfaces of MOSFETs 30 and 31 and the gate electrodes 30″ and 31″ on the same surfaces are then wire bonded to selected ones of the lead frame pins. Thus, sets of wire bonds connect the source electrode of die 30 to pins 22 and 23 while the gate electrode of die 30 is wire-bonded to pin 26.

Paragraph number [0031] at page 6:

[0031] In Figures 5, 6 and 7, parts identical to these of Figures 1 to 4 have the same identifying numeral. The IC die 50 is connected to the bottom of pad 21 by an insulation adhesive 51 (Figure 5) such as a polyimide or the like. The IC can derive its operating power from leads 23 and 27 and has a control input terminal connected to pin 26 and an output line 52 which is internally wire bonded to the gate electrode of die 30. The source electrode 30′ of die 30 may be wire bonded to one or more of pins 22 to 25.

CLAIMS:

1. (Amended) A semiconductor device package comprising a lead frame having a conductive pad section with first and second opposite surfaces and a plurality [a] of coplanar pin sections, a first and at least a second semiconductor die, each having first and second opposite surfaces [and each] at least one of said surfaces having a plurality of electrodes; said first [electrodes] surface of [each of] said first [and second] die being fixed to and [in surface to surface connection] connected with said first [and second opposite surfaces respectively] surface of said pad section; said first surface of said second die being fixed to and connected with said second surface of said pad section; [said first and second die being in spacial overlapping relationship with respect to one another; and] an insulation housing enclosing said die and said pad section; a conductive adhesive for connecting said first surface of said first die to said first surface of said pad section; a second adhesive for connecting said first surface of said second die to said second surface of said pad section; wherein said second adhesive is electrically insulative; and wherein said pin [section extending] sections extend through the surface of said insulation housing to its exterior.

6. (Amended) The device of claim [3] 1, wherein selected ones of said plurality of electrodes are connected to selected ones of said plurality of pins within said insulation housing

9. (Amended) The package of claim 2, wherein said first and second die are MOSgated power devices; and wherein said first surfaces of said first and second die each [contain] contains a power electrode to be connected to said pad section and to one another.